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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,755	05/19/2005	Juergen Schroeder	DE02 0279 US	7822
65913	7550	12/12/2008	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			WRIGHT, BRYAN F	
			ART UNIT	PAPER NUMBER
			2431	
			NOTIFICATION DATE	DELIVERY MODE
			12/12/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/535,755

Applicant(s)

SCHROEDER ET AL.

Examiner

BRYAN WRIGHT

Art Unit

2431

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 September 2008.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-14 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-946)
3) ☐ Information Disclosure Statement(s) (PTO/SG/08)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

1. Claim 1 and 10 are amended. Claim 11 – 14 are added. Claims 1-14 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen (EP 0690370 A2).
3. As to claim 1, Cohen teaches a microcontroller the programming of which is carried out in at least one machine-dependent assembler language in which the assembler commands, with the exception of conditional program jumps or program branches (i.e., robust jump [pg. 9, 10-25]), respectively, can be executed in essence independently of data, characterized by at least one random number generator (i.e., pseudo random generator [claim 10]) assigned to the microcontroller can be executed (claim 10), by means of which the program jumps or program branches (i.e., robust jump [claim 9]) can be executed in dependence on the state of the random number generator and/or independently of the internal state of the programming of the microcontroller value prior to ending the instruction (i.e., ... teaches conditionbit and RequestJump parameter to robust jump program [pg. 9, 10-25] such that both parameter are derived by a pseudo random generator signal [claim 10]).

4. As to claim 2, Cohen teaches a microcontroller, characterized by at least one, in particular bit-addressable (i.e., a 8-bit addressable register [fig. 6]), random number register (i.e., load clock division register) assigned to the random number generator (i.e., .. teaches a pseudo random number generator [claim 10] controlled by a clock division register [430, fig. 4]).
5. As to claim 3, Cohen teaches a microcontroller, characterized by an embodiment as a smartcard controller smartcard controller including the microcontroller of claim 1 (i.e., ... teaches 7916 device Note: A smart card is inherently a microprocessor. [pg. 4, lines 40-45]).
6. As to claim 4, Cohen teaches a electrical or electronic device controlled by means of at least one microcontroller (i.e., teaches a microcode controller [pg. 5, lines 20-25]).
7. As to claim 5, Cohen teaches a method for processing the programming of a microcontroller executed in at least one machine-dependent assembler language, the assembler commands, with the exception of conditional program jumps or branches (i.e., ...teaches a robust jump conditional program [pg. 9, lines 10-25]), being executed essentially independently of data, characterized in that the program jumps or program branches (i.e., robust jump [claim 9]) are executed in dependence on the state of at least one random number generator and/or independently of the internal state of the programming of the microcontroller (i.e., ...teaches a random generator operable to generate a signal to execute instruction [claim 10] .. further teaches control algorithm [pg. 12, lines 5-50]).

8. As to claim 6, Cohen teaches a method, characterized in that the random number generated by the random number generator read via software via registers (i.e., clock division register) and the random number read is then evaluated with a conditional program jump or branch (i.e., ... teaches a requestedjump parameter read into robust jump program [pg. 9, lines 10-15]).

9. As to claim 7, Cohen teaches a method, characterized in that, if at least one, in particular bit-addressable (i.e., 8 bit-address register [300, fig. 5]), random number register (i.e., clock division register) is present, testing per bit of the random number register and a conditional jump or branch is carried out (i.e., ... teaches logic for carrying out the conditional jump [pg. 9, 10-25]).

10. As to claim 8, Cohen teaches a method, characterized by the implementation of at least one assembler command ("branch on random bit"), a defined bit of the random number register (i.e., clock division register) being supplied, in particular directly, to the condition input for the conditional jump or branch [pg. 9, lines 10-25].

11. As to claim 9, Cohen teaches a method, characterized in that at least one Arithmetic Logic Unit (ALU) flag controlling the conditional jumps or branches is replaced (i.e., instruction decoder), in particular via the software, by at least one bit of the random number register (i.e., clock division register), so that the conditional jumps or branches corresponding to the bit of the Arithmetic Logic Unit are controlled by the bit of the Random Number Register (i.e., ...teaches a

instruction decoder providing input to perform the robust jump [460, fig. 7] ... further teaches ConditionBits parameter for control logic of the conditional jump [pg. 9, 10-15]).

12. As to claim 10, Cohen teaches a use of a microcontroller for completely concealing the programming running on the microcontroller, so that at least one program running on the microcontroller is unpredictable and non-reproducible for an external observer (i.e., ... teaches a execution unit containing programming logic [74, fig. 4].

13. As to claim 11, Cohen teaches microcontroller comprising: a central processing unit; a memory accessible to the central processing unit, wherein the memory comprises instructions and wherein the central processing unit is configured for:

accessing the instructions, wherein the instructions comprise instruction sequences and where each instruction sequence produces a same result value for a same input value (i.e., ... teaches a sequence of computer instruction [pg. 10- pg. 14]);

receiving a random number associated with an instruction sequence (i.e., ...teaches pseudo-random generator generating a signal to control instruction [claim 10];

receiving the same input value (i.e., ... teaches receiving duplicate input signals [10, fig. 2]) ;

and executing the instruction sequence associated with the random number using the same input value to produce the same result (i.e., ...teaches executing the instruction base on a signal from a pseudo random generator [claim 10].

14. As to claim 12, Cohen teaches microcontroller where the instructions further comprise a jump instruction (i.e., robust jump [pg. 9]) subject to a condition which if true directs the central processing unit to a program address (i.e., ... teaches jump instruction to machine locations [claim 9]), wherein the instruction sequence is located at the program address (i.e., ...teaches location, and wherein the random number is associated with the instruction sequence via the program address.

15. As to claim 13, Cohen teaches microcontroller where the instructions further comprise a jump instruction (i.e., robust jump [pg. 9])subject to a condition which if true directs the central processing unit to a program address (i.e., ... teaches jump instruction to machine locations [claim 9]), wherein the instruction sequence is located at the program address, and wherein the random number is associated with the instruction sequence via the condition (i.e., ... teaches a pseudo random generator operable to generated a signal to control instruction [claim 10]).

16. As to claim 14, Cohen teaches microcontroller where the random number (i.e., random number signal [claim 10]) is generated by a random number generator (i.e., teaches a pseudo random generator) assigned to the microcontroller [claim 10].

Response to Arguments

17. Examiner withdraws claim 10 objection in view of applicant's amendment.

18. Examiner withdraws objection to drawings under 37 CFR 1.83(a) citing applicant's submittal of formal drawing on 9/4/2008.

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Applicant's arguments, see Amendment /Req. Reconsideration, filed 9/4/2008, with respect to the rejection(s) of claim(s) 1-10 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Cohen (EP 0690370 A2).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRYAN WRIGHT whose telephone number is (571)270-3826. The examiner can normally be reached on 8:30 am - 5:30 pm Monday -Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AYAZ Sheikh can be reached on (571)272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BRYAN WRIGHT/

Examiner, Art Unit 2431

/Kimyen Vu/

Supervisory Patent Examiner, Art Unit 2435